

NANO EXPRESS

Open Access



A Study on the Effect of the Structural Parameters and Internal Mechanism of a Bilateral Gate-Controlled S/D Symmetric and Interchangeable Bidirectional Tunnel Field Effect Transistor

Xiaoshi Jin^{1*} , Yicheng Wang¹, Kailu Ma¹, Meile Wu¹, Xi Liu¹ and Jong-Ho Lee²

Abstract

A bilateral gate-controlled S/D symmetric and interchangeable bidirectional tunnel field effect transistor (B-TFET) is proposed in this paper, which shows the advantage of bidirectional switching characteristics and compatibility with CMOS integrated circuits compared to the conventional asymmetrical TFET. The effects of the structural parameters, e.g., the doping concentrations of the N⁺ region and P⁺ region, length of the N⁺ region and length of the intrinsic region, on the device performances, e.g., the transfer characteristics, I_{on}/I_{off} ratio and subthreshold swing, and the internal mechanism are discussed and explained in detail.

Keywords: Tunnel field effect transistor, CMOS, Bidirectional switch, Subthreshold swing, Nanoscale

Introduction

Power consumption is one of the main problems of the integrated circuit industry. If a device works in the on state, its conduction current must reach a certain critical value; when the current reaches a critical value, the corresponding gate voltage is defined as the threshold voltage. When the device is in the off state, the corresponding gate voltage should be a different value from that in the critical on state, which is often called the off-state voltage. The concept of subthreshold swing (SS) is applicable to the device that operates between the off state and the critical on state, which is equal to the change in gate voltage when the current increases by an order of magnitude. When the device is well designed, the critical on-state current value, threshold voltage and off-state

voltage of the device have been determined; then, a smaller SS corresponds to stronger current changes in the subthreshold area, a smaller static current of the device in the off state, and lower static power consumption of the device. The SS of metal oxide semiconductor field effect transistors (MOSFETs), which are the basic unit cells widely used in integrated circuits, is limited by the physical mechanism of the current generated while the device is working and cannot be lower than the limit value of 60 mV/dec. To breakthrough this limitation, a tunnel field effect transistor (PIN or NIP TFETs) based on silicon-based technology has been proposed in recent years. A conventional TFET is formed by adding a layer of low doping intrinsic semiconductors between *p*- and *n*-type semiconductor materials. Compared with MOSFET, the TFET has the advantages of high sensitivity and low static power consumption [1]. TFET is switched by modulating quantum tunneling through a barrier instead of modulating the thermionic emission over a barrier as in the traditional MOSFET. Thus, TFET is not limited by

*Correspondence: xsjin@live.cn

¹ School of Information Science and Engineering, Shenyang University of Technology, Shenyang 110870, China

Full list of author information is available at the end of the article

the thermal Maxwell–Boltzmann tail of carriers, which limits the SS of MOSFET to 60 mV/dec at room temperature [2] (exactly 63 mV/dec at 300 K). The concept was proposed by Chang et al. while working at IBM [3]. For the first time, Joerg Appenzeller and his colleagues at IBM demonstrated that the SS of TFET could be lower than 60 mV/dec. TFET can be used as energy-efficient electronic switches [4], which breaks through the bottleneck of MOSFETs and greatly reduces the IC power consumption. The production process is compatible with MOSFETs. It is likely to replace the MOSFET transistor as the basic unit of next-generation integrated circuits. Therefore, TFETs have become a hot topic in recent years [5, 6]. To improve the performance of TFETs in terms of SS, forward conducting current and reverse leakage, many studies on the structure design and optimization of TFET devices have been conducted, which mainly focus on improving the structure shape of the device channel and gate electrode [7–12] and the gate dielectric materials with different work functions. The characteristic analysis and structure optimization of the gate dielectric material [13–15] and gate dielectrics with different dielectric constants have been performed [15–20]. In device physics, the analytical modeling of TFETs with the double-gate structure [21–27] and surrounding-gate structure [28–33] has also been extensively performed. One disadvantage of silicon-based TFETs compared to MOSFETs is the smaller forward current, and the magnitude of the forward current is determined by the efficiency of the tunneling current generation. The tunneling current generation efficiency can be increased by reducing the band gap between valence band and conduction band in the region that is used to generate the band-to-band tunneling current or by reducing the thickness of the tunneling region. Therefore, in material engineering, TFET devices based on narrow-band gap semiconductor materials and heterojunction tunneling structures have been extensively developed [34–38]. Meanwhile, the introduction of two-dimensional materials into TFETs as tunneling layers with ultrathin thickness has been extensively studied [39–44]. In addition, some papers have reported the reliability of TFETs, such as the effect of source doping on tunneling band gap interleaving [45], the effect of trap-assisted tunneling on the subthreshold characteristics of TFETs [46], and the effect of random doping on the device performance perturbation [47]. However, the current research results mainly aim at the basic working characteristics and working principles of single TFETs, and the most important fundamental purpose of

the research and development of TFETs is to provide a basic structural unit with lower power consumption and replace the existing MOSFET structure. To achieve this fundamental goal, it must be set in a specific circuit to verify its compatibility with MOSFET technology. At present, research on the circuit design strategy based on TFET devices is gradually conducted, such as the analog and mixed signal circuit [48–50], digital logic circuit [50, 51], power management circuit design [52]. There are also studies on the design of hybrid circuits based on MOSFETs and TFETs [53]. However, the doping types of the source region and drain region are opposite to each other, which creates an asymmetry of source region and drain region. This asymmetric structure makes it impossible to completely replace MOSFET with the source/drain symmetry.

Take the n -type TFET as an example. The side with p -type impurity is used as the source region, while the other side with n -type impurity is used as the drain region. When the device works, a positive potential difference must be applied from the drain region to the source region. If the source electrode and drain electrode are interchanged, i.e., the p -type impurity region is set at a higher potential relative to the n -type impurity region, then the PN junction formed by the p -type impurity region and n -type impurity region will always be in the positive bias state, which causes the failure of the control function of the gate electrode, the TFET will be almost always in the on state and cannot be turned off. In other words, it causes the failure of the TFET switch function. In other words, the circuit functional modules (such as transmission gates), which must use the bidirectional switching characteristics of transistors to work normally, are difficult to realize using conventional TFETs with an asymmetrical structure of source and drain, in order to solve these problems, we proposed a source drain symmetric and interchangeable bidirectional TFET (B-TFET) [54], which shows the advantage of bidirectional switching characteristics and compatibility with CMOS integrated circuits compared to the traditional asymmetrical TFETs. In this paper, we proposed a modified bilateral gate-controlled B-TFET with a planar channel. The effects of key structural parameters, such as the doping concentrations of the N^+ region and P^+ region, length of the N^+ region and length of the intrinsic region, on the device performances, e.g., the transfer characteristics, $I_{on}-I_{off}$ ratio and subthreshold swing, are explained in detail based on physical analysis. Thereafter, these key structural parameters are optimized.

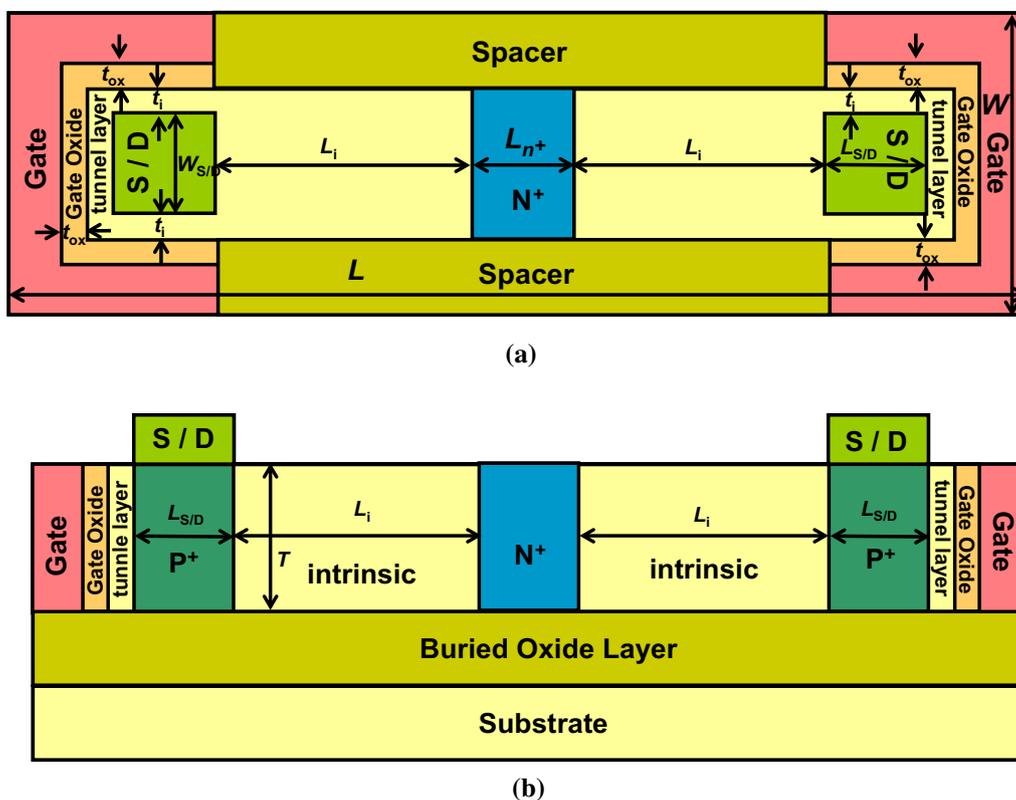


Fig. 1 **a** Schematic top view of the bilateral gate-controlled N-Type B-TFET with planar channel. **b** Cross-view of the bilateral gate-controlled N-Type B-TFET

Methods

Figure 1a shows a schematic top view of the bilateral gate-controlled N-Type B-TFET with a planar channel. Figure 1b shows a cross-view of the bilateral gate-controlled N-Type B-TFET. Unlike the conventional TFET, the proposed B-TFET is completely symmetric, the source/drain interchangeable P^+ -doped regions lay on each side of the silicon body, and the gate electrode lays on both sides of the silicon body. The entire device structure is symmetric. The N^+ -doped region is in the central part of the silicon body. L and W are the entire length and entire width of the proposed device, respectively. L_i is the length of the intrinsic region; L_{N^+} is the length of the N^+ region; $L_{S/D}$ and $W_{S/D}$ are the length and width of the P^+ source/drain interchangeable regions, respectively; T is the silicon body thickness; t_{ox} is the thickness of the gate oxide; t_i is the thickness of the intrinsic tunnel region between S/D region and gate oxide.

In this paper, all physical models such as the Fermi statistical model, CVT mobility model, Auger recombination model, band-gap-narrowing model and a standard band-to-band tunneling model are turned on. All parameters of the device in this paper are listed in Table 1.

Results and Discussion

Figure 2a, b show the transfer characteristic, $I_{on}-I_{off}$ ratio and average SS with different N_D ($10^{18}-10^{21} \text{ cm}^{-3}$). In Fig. 2a, N_D affects the intensity of the reversely biased drain-to-source leakage current. With the increase in doping concentration, the leakage current is significantly suppressed, and the forward current does not significantly change. In Fig. 2b, the SS and $I_{on}-I_{off}$ are also affected by N_D . With the increase in doping concentration, because the reverse leakage current is significantly suppressed, the current at the static operating point decreases, so the average SS also decreases. Because the forward current is much less affected than the reverse

Table 1 Adopted device parameters

Parameters	Values
Body thickness (T)	100 nm
Gate oxide thickness (t_{ox})	1 nm
The thickness of the tunnel region (t_i)	0.5 nm
The entire width of the proposed B-TFET (W)	13 nm
The length of the S/D interchangeable regions ($L_{S/D}$)	8 nm
S/D region width ($W_{S/D}$)	8 nm
N ⁺ -doped region length (L_{N+})	From 2 to 160 nm
The length of the intrinsic region between N ⁺ -doped region and P ⁺ -doped region (L_i)	From 4 to 100 nm
The thickness of the buried oxide layer	50 nm
Doping concentration of P ⁺ region (N_A)	From 5×10^{18} to 1×10^{21} cm ⁻³
Doping concentration of N ⁺ region (N_D)	From 5×10^{18} to 1×10^{21} cm ⁻³
Drain to source voltage (V_{ds})	0.5 V
Gate to source voltage (V_{gs})	From -0.4 to 1 V

leakage, the $I_{on}-I_{off}$ ratio increases with the increase in doping concentration. Figure 2c, d show the 2-dimensional potential distributions of the proposed B-TFET with N_D equal to 10^{19} cm⁻³ and 10^{21} cm⁻³, respectively. When the gate electrode is reversely biased, a strong electric field will be generated between the forward biased drain electrode and the reverse biased gate electrode, which results in a strong band-to-band tunneling near the drain region. Among the resulting generated electron-hole pairs, the electrons can directly flow out of the drain electrode, while the valence band holes must flow through the N⁺ region, subsequently to the intrinsic region in the source side and be discharged by the source electrode to form the continuous leakage current. To minimize the leakage current, the holes produced by band-to-band tunneling should be effectively blocked from flowing out of the N⁺ region. Compared with the N⁺ region with lower concentration, the N⁺ region with higher concentration forms a larger potential difference between P⁺ region and N⁺ region, i.e., the potential value at the boundary between the intrinsic region and the N⁺ region will increase with the increase in N_D because the N⁺ region with higher concentration can produce a larger electronic concentration difference between source and drain. Then, more electrons can be diffused from the N⁺ region to the intrinsic regions on both sides of the N⁺ region, which increases the amount of positive charge (mainly composed of donor) in the N⁺ region after ionization and consequently increases the potential difference between the P⁺ region and N⁺ region. Precisely because the N⁺ region with higher

doping concentration has a higher potential than both the source and drain sides after ionization, the holes generated by the band-to-band tunneling near the drain region can be more effectively blocked, which more effectively decreases the leakage current.

In addition to the doping concentration of the N⁺ region, another key parameter of the N⁺ region, which can significantly affect the reversely biased leakage current, is the length of the N⁺ region. Figure 3a, b show the $I_{ds}-V_{gs}$ transfer characteristics of the proposed B-TFET with different L_{N+} . The reversely biased leakage current largely decreases with increasing L_{N+} . As Fig. 2b shows, the subthreshold swing and $I_{on}-I_{off}$ are also affected by L_{N+} . With the increase in L_{N+} , because the reverse leakage current is significantly suppressed, the current at the static operating point and average SS are also reduced. The forward current is far less affected than the reverse leakage, and the $I_{on}-I_{off}$ ratio increases with the increase in L_{N+} . Figure 3c, d show the 2-dimensional hole concentration distribution of the proposed B-TFET with L_{N+} equal to 2 nm and 80 nm, respectively. When L_{N+} is equal to 2 nm, the minimal hole concentration in the N⁺ region is larger than 10^{17} cm⁻³, while when L_{N+} is equal to 80 nm, the minimal hole concentration is less than 10^{14} cm⁻³. The increase in length of the N⁺ region enhances its ability to prevent holes from passing through the N⁺ region. As a non-equilibrium minority carrier in the N⁺ region, when the N⁺ region is longer, more holes will be recombined with electrons before passing through the N⁺ region, so the increase in length of the N⁺ region can also form a continuous reversely biased leakage

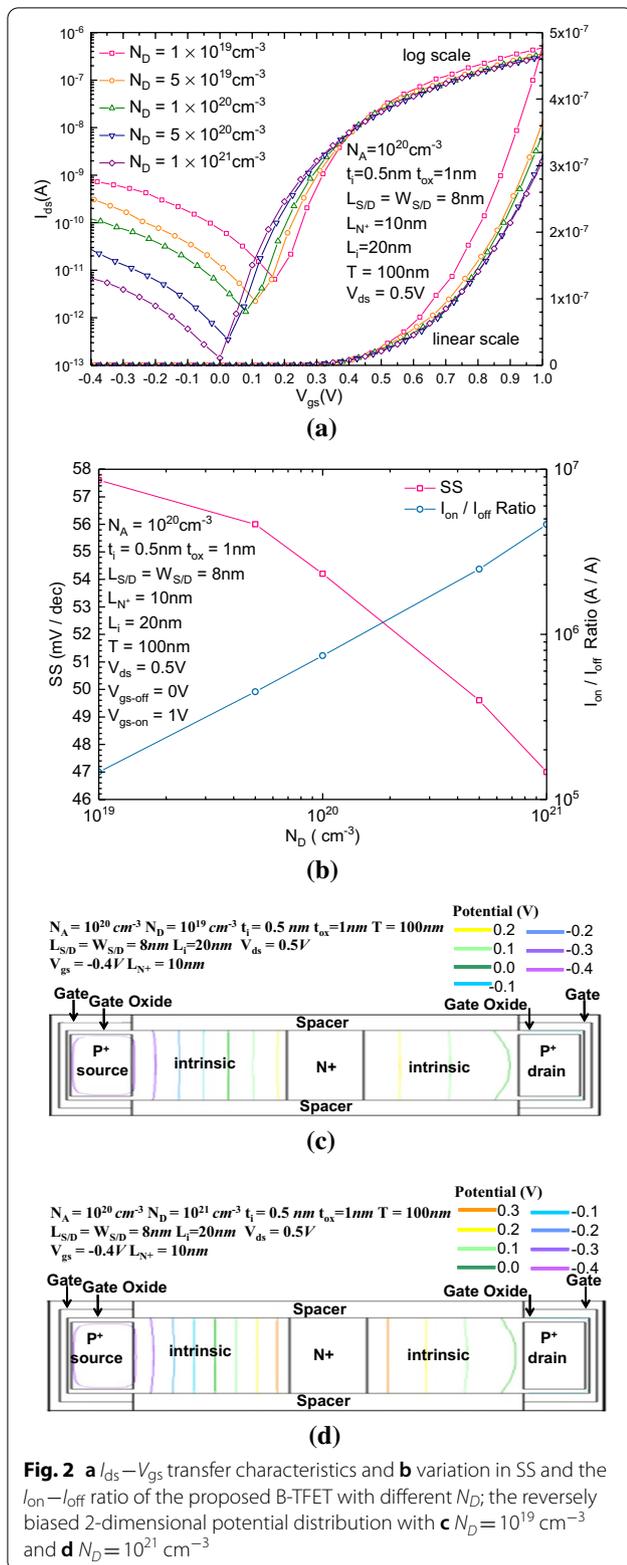


Fig. 2 **a** $I_{ds}-V_{gs}$ transfer characteristics and **b** variation in SS and the $I_{on}-I_{off}$ ratio of the proposed B-TFET with different N_D ; the reversely biased 2-dimensional potential distribution with **c** $N_D = 10^{19} \text{ cm}^{-3}$ and **d** $N_D = 10^{21} \text{ cm}^{-3}$

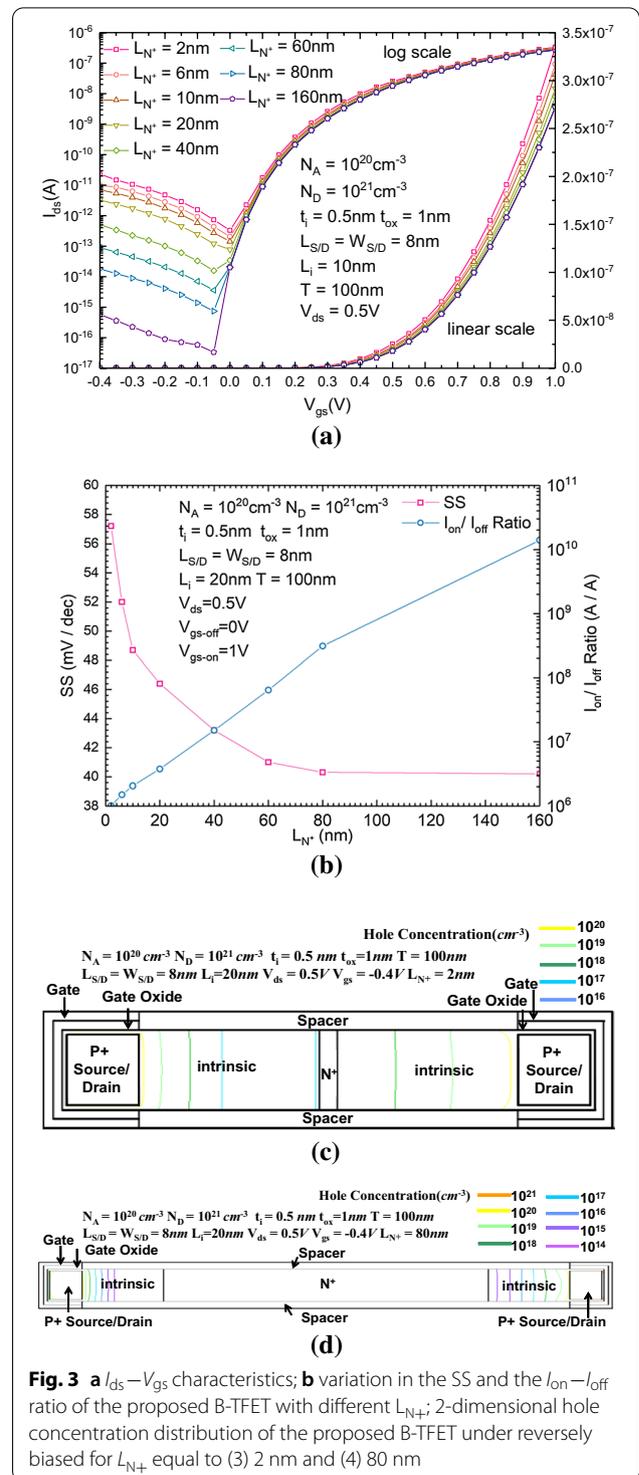
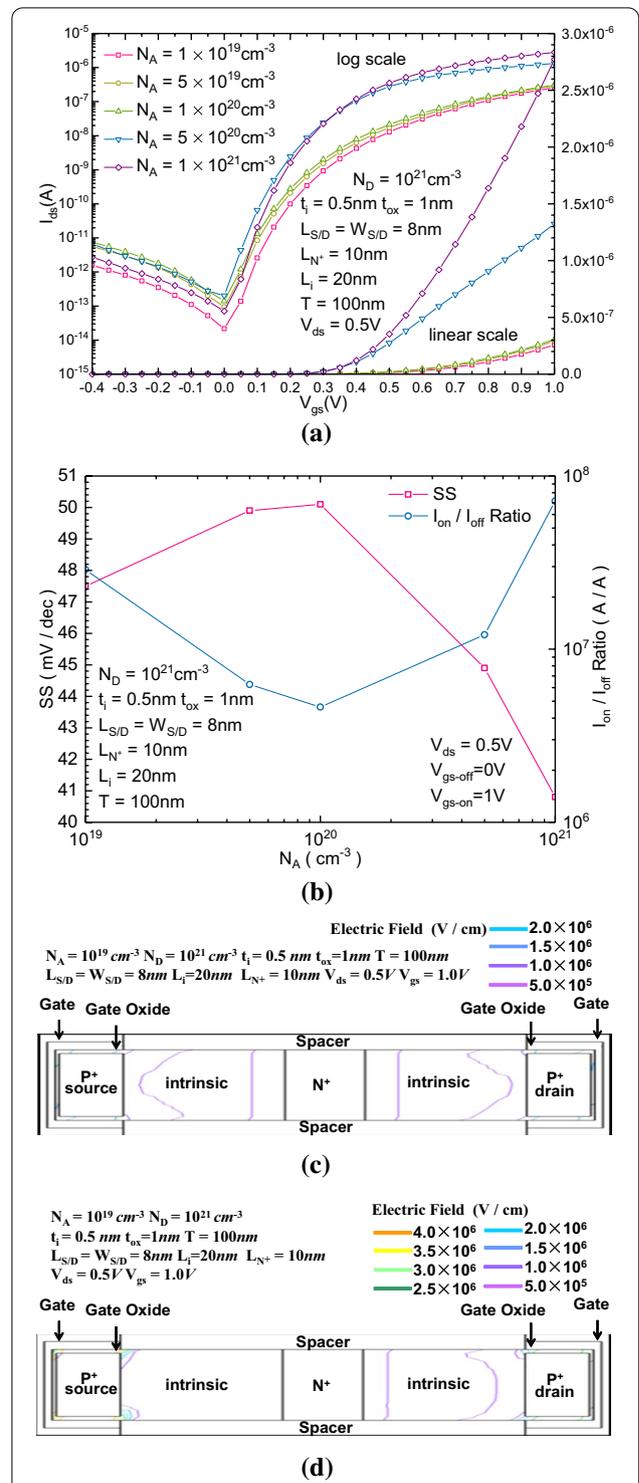
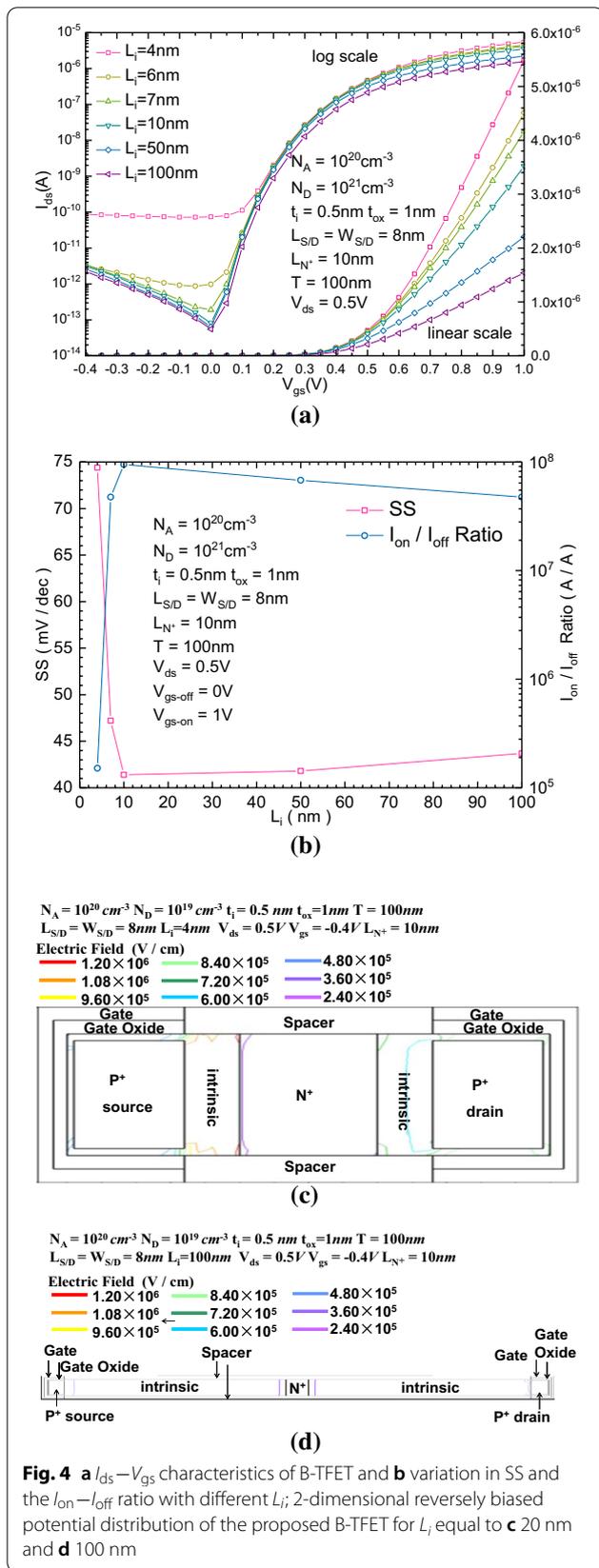


Fig. 3 **a** $I_{ds}-V_{gs}$ characteristics; **b** variation in the SS and the $I_{on}-I_{off}$ ratio of the proposed B-TFET with different L_{N^+} ; 2-dimensional hole concentration distribution of the proposed B-TFET under reversely biased for L_{N^+} equal to (3) 2 nm and (4) 80 nm



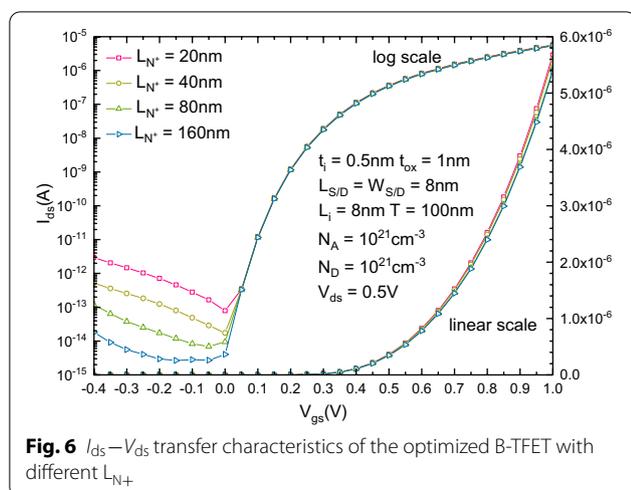


Fig. 6 $I_{ds}-V_{ds}$ transfer characteristics of the optimized B-TFET with different L_{N+}

current. The average SS can be reduced to 40.2 mV/dec, and the $I_{on}-I_{off}$ ratio can exceed 10^{10} .

Figure 4a, b show the $I_{ds}-V_{gs}$ transfer characteristics and changes in SS and $I_{on}-I_{off}$ ratio of the proposed B-TFET with different L_i , respectively. The forward current decreases with increasing L_i because the resistance of the intrinsic region is proportional to the length of itself. Then, to maximize the forward current, the length of the intrinsic region should be minimized. However, the decrease in length of the intrinsic region enhances the electric field in the intrinsic region between the source P+ region and the N+ region, so the band bending near this region is larger than the intrinsic region near the drain electrode, which induces more reversely biased leakage current. Figure 4c, d show the 2-dimensional reversely biased potential distribution of the proposed B-TFET for L_i equal to 4 nm and 100 nm, respectively. For the shortest L_i (4 nm) case, the electric field in the intrinsic region between the source P+ region and the N+ region near the source electrode is much stronger than that in the intrinsic region between the drain P+ region and the N+ region near the drain electrode. Then, the leakage current almost remains constant, which is independent of the change in gate voltage. Figure 4b shows that the optimal value range of L_i is approximately 7–10 nm, where the SS decreases to a valley value of 41 mV/dec and the $I_{on}-I_{off}$ ratio increases to a maximum value of almost 10^8 .

Figure 5a, b show the $I_{ds}-V_{ds}$ transfer characteristics and change in SS and $I_{on}-I_{off}$ ratio of the proposed B-TFET with different N_A . Figure 5a shows that by increasing the concentration of the P+ -doped region, we can obtain less SS and a larger forward current. The reversely biased leakage current is not obviously affected by the change in N_A , but the forward current can be increased with the increase in N_A . In Fig. 5b, both SS and $I_{on}-I_{off}$ ratio can be improved by increasing N_A . Figure 5c, d show the 2-dimensional electric field distribution of the proposed B-TFET with N_A equal to 10^{19} cm^{-3} and 10^{21} cm^{-3} , respectively. The increase in N_A enhances the electric field in the intrinsic tunnel region; then, more electron- hole pairs can be generated through band-to-band tunneling, which enhances the forward current of the proposed B-TFET.

According to the above discussion, both N_D and N_A should be set to the maximal possible value. The optimal value range of L_i is 7–10 nm. However, there is a tradeoff between the static power consumption and L_{N+} . Figure 6 shows the $I_{ds}-V_{ds}$ transfer characteristics of the optimized B-TFET with different L_{N+} . L_{N+} can be selected according to different static power consumption design requirements. As a compromise, to ensure that the $I_{on}-I_{off}$ ratio is above 10^8 , L_{N+} is recommended to be above 20 nm. The on current is increased to approximately $6 \times 10^{-6} \text{ A}$, and the SS is reduced to 38 mV/dec.

Conclusions

In this paper, the effects of the structural parameters and internal mechanism of a bilateral gate-controlled S/D symmetric and interchangeable bidirectional tunneling field effect transistor are analyzed. The effects of the key parameters such as the concentration and length of the N+ region, length of the intrinsic region between the P+ and N+ regions, and concentration of the P+ region have been discussed in detail. Compared with the conventional TFET, the B-TFET has the advantage of strong resistance to the reversely biased leakage current. Thereafter, good performance such as a lower average SS and a higher $I_{on}-I_{off}$ ratio can be obtained. Moreover, due to the structural symmetry and source/drain interchangeable and bidirectional switching characteristics, it is more compatible with the CMOS circuit.

Abbreviations

L : Entire length of the proposed device; W : Entire width of the proposed device; L_i : Length of the intrinsic region; L_{N+} : Length of the N^+ region; $L_{S/D}$: Length of the P^+ source/drain interchangeable regions; $W_{S/D}$: Width of the P^+ source/drain interchangeable regions; T : Silicon body thickness; t_{ox} : Thickness of the gate oxide; t_i : Thickness of the intrinsic tunnel region between S/D region and gate oxide; MOSFET: Metal oxide semiconductor field effect transistor; TFET: Tunnel field effect transistor.

Acknowledgements

This work is supported by the Natural Science Foundation of Liaoning Province No. 2019-MS-250.

Authors' contributions

All sections of the manuscript are contributed by all authors in the list of authors. XJ contributed to manuscript writing and theoretical guidance. YW contributed to simulation and data analysis. MW contributed to data analysis, sorting and figure editing. XL was involved in manuscript writing and theoretical guidance. J-HL contributed to technical discussion and theoretical guidance. All authors read and approved the final manuscript.

Authors' information

Xiaoshi Jin, received a B.S. degree in physics from Dalian University of Technology, Dalian, China, in 2004, an M.S. degree in physics from Gyeongsang National University, Jinju, Korea, in 2006 and a Ph.D. degree in semiconductor and display engineering from Kyungpook National University, Daegu, Korea, in 2010. He works in the School of Information Science and Engineering, Shenyang University of Technology as an associate professor. He has authored or coauthored more than 40 papers published in refereed journals and has been granted more than 40 patents in this area. His research interests include semiconductor physics, device modeling, and design of advanced semiconductor devices and ICs.

Yicheng Wang, is currently working toward an M.S. degree in the School of Information Science and Engineering, Shenyang University of Technology, Shenyang, China. His research interests include the design and optimization of advanced TFETs.

Kailu Ma, is currently working toward an M.S. degree in the School of Information Science and Engineering, Shenyang University of Technology, Shenyang, China. Her research interests include the design and optimization of advanced TFETs.

Meile Wu, received a Ph.D. degree in Electrical and Computer Engineering, Seoul National University, Korea. She works in the School of Information Science and Engineering, Shenyang University of Technology as an assistant professor. Her research interests include the design of advanced semiconductor devices and gas sensors.

Xi Liu, received B.S. and M.S. degrees in applied mathematics from Dalian University of Technology, Dalian, China, in 2004 and 2006, respectively. She received a Ph.D. degree in semiconductor and display engineering from Kyungpook National University, Daegu, Korea, in 2010. She works in the School of Information Science and Engineering, Shenyang University of Technology as an associate professor. Her research interests include the design and optimization of advanced integrated circuits and semiconductor devices.

Jong-Ho Lee, received a Ph.D. degree in electronic engineering from Seoul National University, Seoul, in 1993. In 1994, he was at the School of Electrical Engineering, Wonkwang University, Iksan, Chonbuk, Korea. In 2002, he moved to Kyungpook National University, Daegu, Korea, as a Professor of the School of Electrical Engineering and Computer Science. Since September 2009, he has been a Professor in the School of Electrical Engineering, Seoul National University, Seoul, Korea. From August 1998 to July 1999, he was at Massachusetts Institute of Technology, Cambridge, as a postdoctoral fellow. He has authored or coauthored more than 200 papers published in refereed journals and over 280 conference papers related to his research and has been granted more than 100 patents in this area. His research interests include CMOS technology, nonvolatile memory devices, thin-film transistors, sensors, bio-interface, and neuromorphic technology. He has served as a subcommittee member of IEDM, ITRS ERD member, a general chair of IPFA2011, and IEEE EDS Korea

chapter chair. In 2006, he received the "This Month's Scientist Award" for his contribution in the development of practical high-density/high-performance 3-dimensional nanoscale CMOS devices. He invented the Saddle FinFET (or recess FinFET) for the DRAM cell and NAND flash cell string with virtual source/drain, which has been applied for mass production.

Funding

The Natural Science Foundation of Liaoning Province No. 2019-MS-250. This fund is used to pay for the publication of papers.

Availability of data and materials

We included a statement of availability of data and material for ourselves and on behalf of our coauthors under the "Competing interests". All available data and material are original work. All data have been clearly provided in the manuscript without additional data and supporting materials.

Declaration

Competing interests

The authors declare that they have no competing interests.

Author details

¹School of Information Science and Engineering, Shenyang University of Technology, Shenyang 110870, China. ²School of EECS Engineering and ISRC (Inter-University Semiconductor Research Center), Seoul National University, Shinlim-Dong, Kwanak-Gu, Seoul 151-742, Korea.

Received: 20 December 2019 Accepted: 2 June 2021

Published online: 08 June 2021

References

1. Avci UE, Morris DH, Young IA (2015) Tunnel field-effect transistors: prospects and challenges. *IEEE J Electron Devices Soc* 3(3):88–95
2. DeMicheli G, Leblebici Y, Gijs M, Vörös J (2009) *Nanosystems design and technology*. Springer, Berlin
3. Chang LL, Esaki L (1977) Tunnel triode—a tunneling base transistor. *Appl Phys Lett* 31(10):687–689
4. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* 479(7373):329
5. Wu JZ, Min J, Taur Y (2015) Short-channel effects in tunnel FETs. *IEEE Trans Electron Devices* 62(9):3019–3024
6. Ilatikhameneh H, Klimeck G, Rahman R (2016) Can homojunction tunnel FETs scale below 10 nm? *IEEE Electron Device Lett* 37(1):115–118
7. Kim SW, Kim JH, Liu TK, Choi WY, Park BG (2016) Demonstration of L-shaped tunnel field-effect transistors. *IEEE Trans Electron Devices* 63(4):1774–1778
8. Yang ZN (2016) Tunnel field-effect transistor with an L-shaped gate. *IEEE Electron Device Lett* 37(7):839–842
9. Chen SP, Wang SL, Liu HX, Li W, Wang QQ, Wang X (2017) Symmetric U-shaped gate tunnel field-effect transistor. *IEEE Trans Electron Devices* 64(3):1343–1349
10. Chen CY, Ameen TA, Ilatikhameneh H, Rahman R, Klimeck G, Appenzeller J (2018) Channel thickness optimization for ultrathin and 2-D chemically doped TFETs. *IEEE Trans Electron Devices* 65(10):4614–4621
11. Chen F, Ilatikhameneh H, Tan YH, Klimeck G, Rahman R (2018) Switching mechanism and the scalability of vertical-TFETs. *IEEE Trans Electron Devices* 65(7):3065–3068
12. Woo S, Kim S (2019) Covered source-channel tunnel field-effect transistors with trench gate structures. *IEEE Trans Nanotechnol* 18:114–118
13. Ko E, Lee HJ, Park JD, Shin CH (2016) Vertical tunnel FET: design optimization with triple metal-gate layers. *IEEE Trans Electron Devices* 63(12):5030–5035
14. Lee JC, Ahn TJ, Yu YS (2018) Work-function engineering of source-overlapped dual-gate tunnel field-effect transistor. *J Nanosci Nanotechnol* 18(9):5925–5931
15. Raad B, Nigam K, Sharma D, Kondekar P (2016) Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement. *Electron Lett* 52(9):770–771

16. Ilatikhameneh H, Ameen TA, Klimeck G, Appenzeller J, Rahman R (2015) Dielectric engineered tunnel field-effect transistor. *IEEE Electron Device Lett* 36(10):1097–1100
17. Sahay S, Kumar MJ (2015) Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. *IEEE Trans Electron Devices* 62(11):3882–3886
18. Madan J, Chaujar R (2016) Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. *IEEE Trans Device Mater Reliab* 16(2):227–234
19. Raad BR, Nigam K, Sharma D, Kondekar PN (2016) Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement. *Superlattices Microstruct* 94:138–146
20. Rahimian M, Fathipour M (2017) Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric. *Mater Sci Semicond Process* 63:142–152
21. Bagga N, Sarkar SK (2015) An analytical model for tunnel barrier modulation in triple metal double gate TFET. *IEEE Trans Electron Devices* 62(7):2136–2142
22. Kumar S, Goel E, Singh K, Singh B, Kumar M, Jit S (2016) A Compact 2-D analytical model for electrical characteristics of double-gate tunnel field-effect transistors with a SiO₂/high-k stacked gate-oxide structure. *IEEE Trans Electron Devices* 63(8):3291–3299
23. Kumar S, Goel E, Singh K, Singh B, Singh PK, Baral K, Jit S (2017) 2-D analytical modeling of the electrical characteristics of dual-material double-gate TFETs with a SiO₂/HfO₂ stacked gate-oxide structure. *IEEE Trans Electron Devices* 64(3):960–968
24. Guan YH, Li ZC, Zhang WH, Zhang YF (2017) An accurate analytical current model of double-gate heterojunction tunneling FET. *IEEE Trans Electron Devices* 64(3):938–944
25. Mohammadi S, Khavesh HRT (2017) An analytical model for double-gate tunnel FETs considering the junctions depletion regions and the channel mobile charge carriers. *IEEE Trans Electron Devices* 64(3):1268–1276
26. Kumar S, Singh K, Chander S, Goel E, Singh PK, Baral K, Singh B, Jit S (2018) 2-D analytical drain current model of double-gate heterojunction TFETs with a SiO₂/HfO₂ stacked gate-oxide structure. *IEEE Trans Electron Devices* 65(1):331–338
27. Lu B, Lu HL, Zhang YM, Zhang YM, Cui XR, Lv ZJ, Yang SZ, Liu C (2018) A charge-based capacitance model for double-gate tunnel FETs with closed-form solution. *IEEE Trans Electron Devices* 65(1):299–307
28. Xu WJ, Wong H, Iwai H (2015) Analytical model of drain current of cylindrical surrounding gate p–n–i–n TFET. *Solid-State Electron* 111:171–179
29. Dash S, Mishra GP (2015) A new analytical threshold voltage model of cylindrical gate tunnel FET (CG-TFET). *Superlattices Microstruct* 86:211–220
30. Goswami R, Bhowmick B (2017) An analytical model of drain current in a nanoscale circular gate TFET. *IEEE Trans Electron Devices* 64(1):45–51
31. Jiang CS, Liang RR, Xu J (2017) Investigation of negative capacitance gate-all-around tunnel FETs combining numerical simulation and analytical modeling. *IEEE Trans Nanotechnol* 16(1):58–67
32. Bagga N, Dasgupta S (2017) Surface potential and drain current analytical model of gate all around triple metal TFET. *IEEE Trans Electron Devices* 64(2):606–613
33. Guan YH, Li ZC, Zhang WH, Zhang YF, Liang F (2018) An analytical model of gate-all-around heterojunction tunneling FET. *IEEE Trans Electron Devices* 65(2):776–782
34. Liu MS, Liu Y, Wang HJ, Zhang QF, Zhang CF, Hu SD, Hao Y, Han GQ (2015) Design of GeSn-based heterojunction-enhanced N-channel tunneling FET with improved subthreshold swing and ON-state current. *IEEE Trans Electron Devices* 62(4):1262–1268
35. Lind E, Memisevic E, Dey AW, Wernersson LE (2015) III–V heterostructure nanowire tunnel FETs. *IEEE J Electron Devices Soc* 3(3):96–102
36. Ahish S, Sharma D, Kumar YBN, Vasantha MH (2016) Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping. *IEEE Trans Electron Devices* 63(1):288–295
37. Dubey PK, Kaushik BK (2017) T-Shaped III–V heterojunction tunneling field-effect transistor. *IEEE Trans Electron Devices* 64(8):3120–3125
38. Memisevic E, Svensson J, Lind E, Wernersson LE (2017) InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors. *IEEE Trans Electron Devices* 64(11):4746–4751
39. Roy T, Tosun M, Cao X, Fang H, Lien DH, Zhao PD, Chen YZ, Chueh YL, Guo J, Javey A (2015) Dual-gated MoS₂/WSe₂ van der Waals tunnel diodes and transistors. *ACS Nano* 9(2):2071–2079
40. Szabo A, Koester SJ, Luisier M (2015) Ab-initio simulation of van der Waals MoTe₂–SnS₂ heterotunneling FETs for low-power electronics. *IEEE Electron Device Lett* 36(5):514–516
41. Li M, Esseni D, Nahas JJ, Jena D, Xing HG (2015) Two-dimensional heterojunction interlayer tunneling field effect transistors (thin-TFETs). *IEEE J Electron Devices Soc* 3(3):206–213
42. Sarkar D, Xie XJ, Liu W, Cao W, Kang JH, Gong YJ, Kraemer S, Ajayan PM, Banerjee K (2015) A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* 526(7571):91–95
43. Ameen TA, Ilatikhameneh H, Klimeck G, Rahman R (2016) Few-layer phosphorene: an ideal 2D material for tunnel transistors. *Sci Rep* 6:28515
44. Chen FW, Ilatikhameneh H, Ameen TA, Klimeck G, Rahman R (2017) Thickness engineered tunnel field-effect transistors based on phosphorene. *IEEE Electron Device Lett* 38(1):130–133
45. Min J, Wu JZ, Taur Y (2015) Analysis of source doping effect in tunnel FETs with staggered bandgap. *IEEE Electron Device Lett* 36(10):1094–1096
46. Sajjad RN, Chern W, Hoyt JL, Antoniadis DA (2016) Trap assisted tunneling and its effect on subthreshold swing of tunnel FETs. *IEEE Trans Electron Devices* 63(11):4380–4387
47. Carrillo-Nunez H, Lee J, Berrada S, Medina-Bailon C, Adamu-Lema F, Luisier M, Asenov A, Georgiev VP (2018) Random dopant-induced variability in Si-InAs nanowire tunnel FETs: a quantum transport simulation study. *IEEE Electron Device Lett* 39(9):1473–1476
48. Sedighi B, Hu XS, Liu HC, Nahas JJ, Niemier M (2015) Analog circuit design using tunnel-FETs. *IEEE Trans Circuits Syst I-Reg Pap* 62(1):39–48
49. Settino F, Lanuzza M, Strangio S, Crupi F, Palestri P, Esseni D, Selmi L (2017) Understanding the potential and limitations of tunnel FETs for low-voltage analog/mixed-signal circuits. *IEEE Trans Electron Devices* 64(6):2736–2743
50. Strangio S, Settino F, Palestri P, Lanuzza M, Crupi F, Esseni D, Selmi L (2018) Digital and analog TFET circuits: design and benchmark. *Solid-State Electron* 146:50–65
51. Bi Y, Shamsi K, Yuan JS, Jin Y, Niemier M, Hu XS (2017) Tunnel FET current mode logic for DPA-resilient circuit designs. *IEEE Trans Emerg Top Comput* 5(3):340–352
52. Cavalheiro DN, Moll F, Valtchev S (2018) Prospects of tunnel FETs in the design of power management circuits for weak energy harvesting DC sources. *IEEE J Electron Devices Soc* 6(1):382–391
53. Lanuzza M, Strangio S, Crupi F, Palestri P, Esseni D (2015) Mixed tunnel-FET/MOSFET level shifters: a new proposal to extend the tunnel-FET application domain. *IEEE Trans Electron Devices* 62(12):3973–3979
54. Jin XS, Gao YX, Liu X, Lee JH (2018) A source drain symmetric and interchangeable bidirectional tunneling field effect transistor. *AIP Adv* 8(8):085318

Publisher's Note

Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.